

**Integrated chip package structure using silicon substrate and method of  
manufacturing the same**

Appl. No. : 10/755,042 Confirmation No. 8665  
Applicant : Jin-Yuan Lee,  
Mou-Shiung Lin,  
Ching-Cheng Huang  
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Examiner : Jackson JR, Jerome  
Docket No. : MEGP0004USA1  
Customer No. : 27765

Commissioner for Patents  
P.O. Box 1450  
Alexandria VA 22313-1450

5                   **RESPONSE TO FINAL OFFICE ACTION AND ADVISORY OFFICE  
ACTION**

Sir:

10           In response to the Final Office Action mailed Dec. 10, 2008 and Advisory Office  
Action mailed Mar. 26, 2009, please amend the above-identified application and consider  
the remarks as follows:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2  
of this paper.

**Remarks/Arguments** begin on page 9 of this paper.